AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-18. (Canceled)

19. (Currently Amended) A semiconductor device ~~according to claim 18,~~ comprising:

a functional circuit block for performing a processing when an instruction or data is inputted,

a power status control circuit for controlling a power status of said functional circuit block, and

a prediction circuit coupled to receive the instruction or data for controlling said power status control circuit, independently of other computation devices, based on said instruction or data and on an interval between successive instructions or data which are inputted to both the functional circuit block and the prediction circuit,

wherein said power status control circuit comprises a power shutdown circuit for shutting down power which is supplied to said functional circuit block, said power shutdown circuit being coupled to said functional circuit block and a power supply,

wherein clock pulses are inputted into said functional circuit block and said power status control circuit,

wherein said prediction circuit comprises a counter for counting the number of clock pulses inputted to said functional circuit block and to said counter, a control circuit for controlling said power shutdown circuit, and an input detection circuit receiving the instruction or data inputted to said functional circuit block for detecting said instruction or data inputted to said functional circuit block,

wherein said counter outputs a first signal to said control circuit when a number of said clock pulses counted is n,

wherein, when there is no instruction or data inputted to said functional circuit block, said input detection circuit outputs a reset signal to said counter to reset a counting of said clock pulses and outputs a second signal to said control circuit, and said control circuit outputs an output signal of a first state to shut down said power supplied to said functional circuit block when both said first and second signals are inputted to said control circuit,

wherein said functional circuit block comprises a register for temporarily storing said instruction or data and a functional block for computation, and

wherein said prediction circuit further comprises a comparator for controlling said register by comparing the output of said control circuit with the number of clock pulses inputted to said comparator and a predetermined number, said comparator starting a counting of said clock pulses when said control circuit outputs said output signal of a second state.

20-28. (Canceled)

29. (Previously Presented) A semiconductor device comprising:

a functional circuit block for performing a processing when an instruction or data is inputted,

a power status control circuit for controlling a power status of said functional circuit block, and

a prediction circuit coupled to receive the instruction or data for controlling said power status control circuit, independently of other computation devices, based on said instruction or data which is inputted to both the functional circuit block and the prediction circuit,

wherein said power status control circuit comprises a power shutdown circuit for shutting down power which is supplied to said functional circuit block, said power shutdown circuit being coupled to said functional circuit block and a power supply,

wherein clock pulses are inputted into said functional circuit block and said power status control circuit,

wherein said prediction circuit comprises a counter for counting the number of clock pulses inputted to said functional circuit block and to said counter, a control circuit for controlling said power shutdown circuit, and an input detection circuit receiving the instruction or data inputted to said functional circuit block for detecting said instruction or data inputted to said functional circuit block,

wherein said counter outputs a first signal to said control circuit when a number of said clock pulses counted is n,

wherein, when there is no instruction or data inputted to said functional circuit block, said input detection circuit outputs a reset signal to said counter to reset a

counting of said clock pulses and outputs a second signal to said control circuit, and said control circuit outputs an output signal of a first state to shut down said power supplied to said functional circuit block when both said first and second signals are inputted to said control circuit,

wherein said functional circuit block comprises a register for temporarily storing said instruction or data and a functional block for computation, and

wherein said prediction circuit further comprises a comparator for controlling said register by comparing the output of said control circuit with the number of clock pulses inputted to said comparator and a predetermined number, said comparator starting a counting of said clock pulses when said control circuit outputs said output signal of a second state.